REMARKS

Claims 1-8 and 12-14 are now pending in the application. By this paper, Claims 1, 2, and 12 have been amended and Claims 9 and 10 have been cancelled without prejudice or disclaimer of the subject matter contained therein. The basis for these amendments can be found throughout the specification, claims, and drawings originally filed. No new matter has been added. The preceding amendments and the following remarks are believed to be fully responsive to the outstanding Office Action and are believed to place the application in condition for allowance.

The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

INFORMATION DISCLOSURE STATEMENT

The Examiner has asked Applicant to verify the IDS filed on March 15, 2004 by identifying U.S. Document No. 2002/001162 A1, dated January 31, 2002 in the name of Hidea. Applicant respectfully submits that the document referred to by the Examiner should be U.S. Publication No. 2002/0011612 A1 dated January 31, 2002 to Hidea rather than 2002/001162 A1. The missing number "1" identifying the U.S. Publication to Hidea in the IDS filed on March 15, 2004 was omitted due to a typographical error. The Examiner is respectfully requested to consider U.S. Publication No. 2002/0011612 as properly submitted in the IDS filed March 15, 2004 in light of the foregoing remarks.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 5, 7, 12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Sekido et al. (JP-05-075121).

This rejection is respectfully traversed.

Independent Claim 1 calls for a semiconductor device including a support base, an insulating layer formed on a support base, a semiconductor layer formed on the insulating layer, a source region formed in the semiconductor layer, and a drain region formed in the semiconductor layer. A channel region is formed between the source region and the drain region in the semiconductor layer. A gate insulating layer is formed above the channel region and a gate electrode is formed above the gate insulating layer. The gate electrode has a major axis and a minor axis and first and second ends that are spaced apart along the major axis, overlap the semiconductor layer, and are in contact with the insulating layer. A boundary between the gate insulating layer and a channel region is a wave-like pattern of a gradual slope having crests and troughs alternately spaced apart along the major axis of the gate electrode.

Independent Claim 12 calls for a semiconductor device including a support base, an insulating layer formed on the support base, a semiconductor layer formed on the insulating layer, a source drain region formed in the semiconductor layer, and a drain region formed in the semiconductor layer. A channel region is formed between the source region and the drain region and the semiconductor layer, a gate insulating layer is formed above the channel region, and a gate electrode is formed above the gate insulating layer. The gate electrode has a major axis and a minor axis and first and second ends that are spaced apart along the major axis, overlap the semiconductor

layer, and they are in contact with the insulating layer. A boundary between the gate insulating layer and channel region undulates and includes crests and troughs alternately spaced apart along the major axis of the gate electrode.

Sekido fails to teach a gate electrode including first and second regions that overlap a semiconductor layer and are in contact with an insulating layer. Rather, Sekido teaches a semiconductor device including a substrate (11), a source region (16S), a drain region (16D), and a gate electrode (15). See Sekido at FIGS. 2 and 5. The gate electrode extends into a channel region (7) having a series of slots (19) formed therein. See Sekido at FIGS. 1, 2, and 5. The slots extend into the channel filed and include a general triangular shape. See Sekido at FIGS. 1, 2, and 5. Sekido fails to teach an insulating layer disposed generally between a semiconductor device and a supporting substrate. In this manner, Applicant respectfully submits that Sekido cannot teach a gate electrode positioned on a semiconductor device, whereby respective ends of the gate electrode overlap the semiconductor device and are in contact with an insulating layer formed on a support substrate.

Because Sekido fails to teach a gate electrode including first and second regions that overlap a semiconductor layer and are in contact with an insulating layer disposed on a support base, Applicant respectfully submits that Sekido fails to teach each and every element of the present invention. Accordingly, Applicant respectfully submits that independent Claims 1 and 12, as well as Claims 5 and 7, respectfully dependent therefrom, are in condition for allowance. Therefore, reconsideration and withdrawal of the rejection if respectfully requested.

REJECTION UNDER 35 U.S.C. § 103

Claims 2-4, 6, 8, and 13-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sekido et al. (JP-05-075121).

Claims 9-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Sekido et al. (JP-05-075121) in view of Ker et al. (U.S. Patent No. 6,750,515).

These rejections are respectfully traversed.

At the outset, Applicant respectfully submits that this rejection is moot with respect to Claims 9 and 10, as Claims 9 and 10 have been cancelled without prejudice. Accordingly, reconsideration and withdrawal of the rejection is respectfully requested.

In addition to the foregoing, Applicant respectfully submits that this rejection is similarly moot with respect to Claims 3, 5, 13, and 14 as Claims 3, 5, 13, and 14 respectfully depend from independent Claims 1, and 12, which are believed to be in condition for allowance in light of the foregoing remarks. Accordingly, reconsideration and withdrawal of the rejections is respectfully requested.

Independent Claim 2 calls for a semiconductor device including a support base, an insulating layer formed on the support base, a semiconductor layer formed on the insulating layer, a source region formed in the semiconductor layer, and a drain region formed in the semiconductor layer. A channel region is formed between the source region and the drain region in the semiconductor layer, a gate insulating layer is formed above the channel region, and a gate electrode is formed above the gate insulating layer. The gate electrode includes a major axis and a minor axis and first and second ends that are spaced apart along the major axis, overlap the semiconductor layer, and are in contact with the insulating layer. A boundary between the gate insulating layer

and the channel region is a wave-like pattern without any corners, with the wave-like pattern having crests and troughs alternately spaced apart along the major axis of the gate electrode.

As described above with respect to independent Claims 1 and 12, Sekido fails to teach an insulating layer disposed between a semiconductor and a substrate and therefore also fails to teach a gate electrode including first and second regions that overlap a semiconductor layer and are in contact with the insulating layer disposed on the substrate. Accordingly, Applicant respectfully submits that Sekido fails to teach or suggest the claimed invention.

Because Sekido does not disclose a gate electrode including first and second regions that overlap a semiconductor layer and are in contact with an insulating layer disposed on a support base, and none of the cited references cures this deficiency on Sekido, Applicant's invention is not taught or suggested by the prior art and reconsideration and withdrawal of the rejection is respectfully requested.

In this manner, it is believed that independent Claim 2, as well as Claims 4, 6, and 8, dependent therefrom are in condition for allowance in light of the art of record. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is

believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Dated: February 17, 2006

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